We claim:

1. A circuit, comprising:

a first filter to filter first components of two differential input signals;

a second filter to filter second components of the differential input signals; and

a delay cell to generate a delayed differential signal based on outputs of the first and second filters.

2. The circuit of claim 1, wherein the first and second filters smooth a state transition in the delayed differential signal, the state transition corresponding to an offset that exists between the differential input signals.

3. The circuit of claim 2, wherein the offset is one of a time offset and phase offset.

4. The circuit of claim 2, wherein the delayed differential signal is a continuous time-varying signal.

5. The circuit of claim 1, wherein the first components are positive components of the differential input signals and the second components are negative components of the differential input signals.

6. The circuit of claim 1, wherein the first filter includes a resistor having a resistance value which smooths a state transition in a first component of the delayed differential signal.

7. The circuit of claim 6, wherein the second filter includes a resistor having a resistance value which smooths a state transition in a second component of the delayed differential signal.

8. The circuit of claim 1, wherein the delay cell includes:

a load;

a current source;

a first switching circuit to connect the current source to the load based on the first filtered components of the differential input signals;

a second switching circuit to connect the current source to the load based on the second filtered components of the differential input signals; and

terminals to output the delayed differential signal generated based on current flowing between the current source and load.

9. The circuit of claim 8, wherein the load includes a symmetric configuration of transistors.

10. A method for generating a delayed signal, comprising:

filtering first components of two differential input signals;

filtering second components of the differential input signals; and

generating a delayed differential signal based on the filtered components of the two differential input signals.

11. The method of claim 10, wherein filtering the first and second components smooths a state transition in the delayed differential signal, the state transition corresponding to an offset between the differential input signals.

12. The method of claim 11, wherein the offset is one of a time offset and phase offset.

13. The method of claim 12, wherein the delayed differential signal is a continuous time-varying signal.

14. The method of claim 10, wherein the first components are positive components of the differential input signals and the second components are negative components of the two differential input signals.

15. The method of claim 10, wherein filtering the first components includes:

coupling the first components of the differential input signals through a first resistor.

16. The method of claim 15, wherein the first resistor has a resistance value which smooths a state transition in a first component of the delayed differential signal.

17. The method of claim 15, wherein filtering the second components includes:

coupling the second components of the differential input signals through a second resistor.

18. The method of claim 17, wherein the second resistor has a resistance value which smooths a state transition in a second component of the delayed differential signal.

19. The method of claim 10, wherein generating the delayed differential signal includes:

connecting a current source to a load based on the first filtered components of the differential input signals;

connecting the current source to the load based on the second filtered components of the differential input signals; and

generating the delayed differential signal based on current flowing between the current source and load.

20. The method of claim 19, wherein the load includes a symmetric configuration of transistors.

21. A delay line, comprising:

a first delay cell which includes a first filter to filter first components of first and second differential signals, a second filter to filter second components of the first and second differential signals, and a delay circuit to generate a delayed differential signal based on outputs of the first and second filters; and

a second delay cell which generates a differential signal which includes the first and second components of the first differential signal input into the first delay cell.

22. The delay line of claim 21, further comprising:

a third delay cell which generates a differential signal which includes the first and second components of the second differential signal input into the first delay cell.

23. The delay line of claim 21, wherein the filters smooth a state transition in the delayed signal, the state transition corresponding to an offset that exists between the first and second differential signals.

24. The delay line of claim 23, wherein the offset is one of a time offset and phase offset.

25. The delay line of claim 21, wherein the filter of the first components includes a resistor having a resistance value which smooths a state transition in a first component of the delayed differential signal.

26. The delay line of claim 25, wherein the second filter includes a resistor having a resistance value which smooths a state transition in a second component of the delayed differential signal.

27. The delay line of claim 21, wherein the first components are positive components of the first and second differential signals and the second components are negative components of the first and second differential signals.

28. A system, comprising:

a first circuit; and

a second circuit including:

a first filter to filter first components of two differential input signals;

a second filter to filter second components of the differential input signals; and

a delay cell to generate a delayed differential signal based on outputs of the first and second filters, the delayed differential signal controlling the first circuit.

29. The system of claim 28, wherein the first circuit includes a chipset.

30. The system of claim 28, wherein the first circuit includes a memory controller.